Unit 5 : Counter and Register

Lesson 1 : Introduction to Counter

1.1. Learning Objectives

On completion of this lesson you will be able to :

- know about counters
- list different types of counters
- discuses the uses of counters
- design asynchronous counter.

Counters are essential to design of advanced circuits found in digital computers. Counters are employed to keep track of a sequence of events. Counters are particularly common in the control and arithmetic units of processor. Counters are used.

- to keep track of the sequence of instructions in a program
- to distribute the sequence of timing signals
- for frequency division for causing time delays
- for counting the number of pulses coming at the input
- for other similar operations.

Counters may count in binary or in non binary fashion.

Counters may count in binary or in non binary fashion. The basic operational characteristics of a counter is sequential, for every present state there is a well defined next state. The design of a counter involves designing combinational logic that decodes the present state and enables entry into the next state of the counting sequence. Counters are generally classified into two groups: synchronous and asynchronous.

Counters are generally classified into two groups: synchronous and asynchronous.

- A synchronous counter has all FFs change state synchronously with the clock input whether a periodic clock or an periodic plus occurs.
- An asynchronous counter is made up of FFs that do not change state simultaneously with the clock input.

In counter, counting direction may up or down and counting mode may be binary or decade.

In counter, counting direction may up or down and counting mode may be binary or decade.

Advantage of asynchronous counter :

- Circuit design is easy
- Minimum number of FF is required, so cost is low

Disadvantage

- Slow speed of operation.
- Operating frequency is low.
- Synchronous counter are faster than the asynchronous counter.

1.2. Asynchronous Ripple Counter

In ripple counter the output of each FF provides the clock signal for the next FF.

We shall now introduce the ripple counters, a basic counter used very commonly because of its simplicity where the clock input are not tied together. In ripple counter the output of each FF provides the clock signal for the next FF. This type of counter is called asynchronous counter because all the FF in ripple counter do not change states in exact synchronism with the clock pulses; only the first FF respond to the clock pulses. The 2nd FF has to wait for the first; to change states before it is toggled (complemented), the third FF has to wait for the 2nd and so no. So, there is a delay between the responses of consecutive FFs. Recall the following points concerning its operation.

- All FFs are first cleared to the 0 state by applying 0 to the direct reset input.
- All T FFs inputs are connected to permanently to logical '1'. The clock pulses are applied only to CK input of the first FF. As a result 1st FF will toggle (change to its opposite state) each time the clock pulses make a regulative i.e. 0 transition.
- The least significant (1st) FF are activated by the system clock and the $1 \rightarrow 0$ transitions of that FF may be used as clock input signal for the next most significant FF. i.e. The output of 1st FF acts the CK input for 2nd FF and so 2nd FF will toggle each time the 1st FF output goes from 1 to 0. Similarly 3rd and 4th FF will toggle when $1 \rightarrow 0$ transition occurs at 2nd FF and 3rd FF respectively. The state of the FF as the incoming pulse arrive are given in the following Table 5.1.

Number of Input pulses	Flip-flop outputs			
	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	0	0	0

Table : 5.1.

From Timing Diagram

The frequency of Q_4 pulse is the $^1/_{16}$ th of the frequency of input clock pulse.

Advantage

- Less expensive

Disadvantage

- Undesirable decoding transient condition.

1.3. Exercise

1.3.1. Multiple choice questions

a) The ripple counter is one kind of

i) sequential counter
ii) asynchronous counter
iii) synchronous counter
iv) up-down counter.

b) Which is the false statement?

i) In an asynchronous counter all FFs changes states at the same time.
ii) In an synchronous counter, all FF changes at the same time.
iii) Counter is of two types
iv) Counter is made up of FF.

c) Which is the false statement?

i) Counters are employed to keep track of a sequence of events
ii) Counters are used to keep track of the sequence of instruction in a program
iii) Counters are used for counting the number of pulses coming at the input
iv) one of the above.

1.3.2. Question for short answers

a) What do you mean by counter?
b) What are the uses of a counter?

1.3.3. Analytical questions

a) How many types of counter are there in this lesson? Describe briefly.
b) Design a 4-bit ripple counter and draw the timing diagram of that counter.

Lesson 2 : Synchronous Counter

2.1. Learning Objectives

On completion of this lesson, you will be able to :

- understand the design and working principle of synchronous counter.

In synchronous counters, all the flip-flops changes state simultaneously and they are capable of operating at higher frequencies.

Synchronous counters are distinguished from asynchronous (or ripple) counters in that the clock pubes in synchronous counters initiate change in the FFs used in the counter. In synchronous counters, all the flip-flops changes state simultaneously and they are capable of operating at higher frequencies. Synchronous counter are generally more complicated and require more logical elements. The following divided-by-10 up counter is an example of synchronous counter.

2.2. Divided by-10 counter

The state diagram of divided by 10 up counter is as follows :

There are 10 states so, so, number of FFs is ld 10 = 4.

State table

The state table of the counter may be obtained as shown in Table 5.2.

Count	Present state	Next state	FF Inputs			
	y_3 y_2 y_1 y_0	y_3 y_2 y_1 y_0	j_3 k_3	j_2 k_2	j_1 k_1	j_0 k_0
0	0 0 0 0	0 0 0 1	0 ×	1 ×	0 ×	1 ×
1	0 0 0 1	0 0 1 0	0 ×	× 0	1 ×	× 1
2	0 0 1 0	0 0 1 1	0 ×	× 1	× 0	1 ×
3	0 0 1 1	0 1 0 0	0 ×	1 ×	× 1	× 1
4	0 1 0 0	0 1 0 1	0 ×	× 0	0 ×	1 ×
5	0 1 0 1	0 1 1 0	0 ×	× 0	1 ×	× 1
6	0 1 1 0	0 1 1 1	0 ×	× 0	× 0	1 ×
7	0 1 1 1	1 0 0 0	1 ×	1 ×	× 1	× 1
8	1 0 0 0	1 0 0 1	× 0	× 0	0 ×	1 ×
9	1 0 0 1	0 0 0 0	× 1	× 1	0 ×	× 1

Table : 5.2.

K-map

The excitation K-maps corresponding to JK FFs are obtained as shown in Fig. 5.1.

	$\bar{y}_1\bar{y}_0$	$\bar{y}_1 y_0$	$y_1 y_0$	$y_1\bar{y}_0$
$\bar{y}_3\bar{y}_2$	0	0	0	0
$\bar{y}_3 y_2$	0	0	1	0
$y_3 y_2$	×	×	×	×
$y_3\bar{y}_2$	×	×	×	×

$J_3 = y_2 y_1 y_0$

	$\bar{y}_1\bar{y}_0$	$\bar{y}_1 y_0$	$y_1 y_0$	$y_1\bar{y}_0$
$\bar{y}_3\bar{y}_2$	×	×	×	×
$\bar{y}_3 y_2$	×	×	×	×
$y_3 y_2$	×	×	×	×
$y_3\bar{y}_2$	0	1	×	×

$K_3 = y_0$

	$\bar{y}_1\bar{y}_0$	$\bar{y}_1 y_0$	$y_1 y_0$	$y_1\bar{y}_0$
$\bar{y}_3\bar{y}_2$	×	×	1	×
$\bar{y}_3 y_2$	×	×	×	×
$y_3 y_2$	×	×	×	×
$y_3\bar{y}_2$	0	0	×	×

$J_2 = y_1 y_1 y_0$

	$\bar{y}_1\bar{y}_0$	$\bar{y}_1 y_0$	$y_1 y_0$	$y_1\bar{y}_0$
$\bar{y}_3\bar{y}_2$	0	1	×	×
$\bar{y}_3 y_2$	0	1	×	×
$y_3 y_2$	×	×	×	×
$y_3\bar{y}_2$	0	0	×	×

$J_1 = y_0\bar{y}_3$

	y_1y_0	$y_1\bar{y}_0$	y_1y_0	$y_1\bar{y}_0$
$\bar{y}_3\bar{y}_2$	0	0	×	0
$\bar{y}_3 y_2$	0	0	1	0
$y_3 y_2$	×	×	×	×
$y_3\bar{y}_2$	×	×	×	×

$K_2 = y_1y_1y_0 = j_2$

	y_1y_0	$y_1\bar{y}_0$	y_1y_0	$y_1\bar{y}_0$
$\bar{y}_3\bar{y}_2$	×	×	1	0
$\bar{y}_3$y2	×	×	1	0
$y_3 y_2$	×	×	×	×
$y_3\bar{y}_2$	0	×	×	×

K1 = $\bar{y}$0

Fig. 5.1 : K-maps corresponding to JK FFS of the counter.

2.3. Exercise

2.3.1. Multiple choice questions

a) In synchronous counters, all the FF

i) do not change state simultaneously
ii) change state simultaneously
iii) reset their inputs
iv) none of the above.

b) Which of the following is capable of operating at higher frequency?

i) asynchronous counter
ii) synchronous counter
iii) register
iv) JK-FF.

2.3.2. Analytical questions

a) Design a divided by 7 up counter.
b) Design a 4-bit binary up counter using JK FFs.

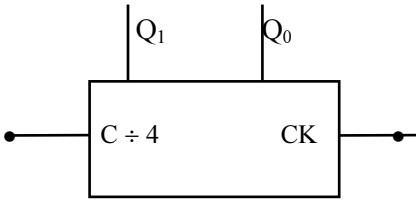
Lesson 3 : Up-down Counter

3.1. Learning Objectives

On completion of this lesson you be able to :

- design up-down counter.

An up down counter is often required which can count in either forward or backward directions depending upon a control signal. When the control signal c=0 then the counter counts upwards (i.e. for divided by 4 up/down counter, it counts 00 $\rightarrow$ 11) but when the control signal c=1, it counts downward direction i.e. for divided by 4 up/down counter, it counts 11 $\rightarrow$ 00. The following is a block diagram of divided by 4 up-down counter.



Up counter is one which counts upward from zero and the down counter is one which counts downward from a maximum count to zero.

The state diagram of this counter is as follows when c = 0, then it acts as up counter when c=1, then it acts as an down counter.

No of state is 4, so, n = 4

$\therefore 2^m >_1 n$

$2^2=4$

2 state variables.

$\therefore$ 2 FF is needed.

The Excitation Table

The excitation table using T FF is as follows

Present state	Next state		FF Inputs			
y_1 y_0	y_1 y_0 c = 0	y_1 y_0 c=1	T_1 c=0	T_1 c=1	T_0 c=0	T_0 c=1
0 0	01	11	0	1	1	1
0 1	10	00	1	0	1	1
1 0	11	01	0	1	1	1
1 1	00	10	1	0	1	1

K-map

The excitation K map corresponding to T FF is as follows :

	$\bar{y}_1\bar{y}_0$	$\bar{y}_1 y_0$	$y_1 y_0$	$y_1\bar{y}_0$
$\bar{c}$	0	1	1	0
c	1	0	0	1

$T_1 = \bar{c}y_0 + c\,\bar{y}_0 = y_0 \oplus c$

	$\bar{y}_1\bar{y}_0$	$\bar{y}_1 y_0$	$y_1 y_0$	$y_1\bar{y}_0$
$\bar{c}$	1	1	1	1
c	1	1	1	1

$T_0 = 1$

$\therefore$ The equation is as follows

$T_1 = \bar{c}y_0 + c\,\bar{y}_0 = y_0 \oplus c$
$T_0 = 1.$

3.2. Exercise

3.2.1. Multiple choice questions

a) Up counter is one which counts

i) downward from a maximum to zero
ii) upward from zero
iii) either upward or downward direction
iv) none of the above.

3.2.2. Question for short answer

a) What is the difference between the counting sequence of an up counter and a down counter?

3.2.3. Analytical question

a) Design a three bit counter that counts up when a control variable E = 0 and counts down when E = 1.

Lesson 4 : Odd Sequence and Down Counters

4.1. Learning Objectives

On completion of this lesson you will be able to :

- design an odd sequence counter
- design and working principle of down counter.

Odd sequence counter

The following odd sequence counter produces the counts sequence.

0 - 3 - 7 - 2 - 5 - 1 - 0

4.2. State Diagram

The state diagram of counter is as follows

The Excitation Table.

Present state	Next state	FF Inputs		
$y_2\ y_1\ y_0$	$y_2\ y_1\ y_0$	$j_2\ k_2$	$j_1\ k_1$	$j_0\ k_0$
0 0 0	0 1 1	0 ×	1 ×	1 ×
0 1 1	1 1 1	1 ×	× 0	× 0
1 1 1	0 1 0	× 1	× 0	× 1
0 1 0	1 0 1	1 ×	× 1	1 ×
1 0 1	0 0 1	× 1	0 ×	× 0
0 0 1	0 0 0	0 ×	0 ×	× 1

K-maps

	$\bar{y}_1\bar{y}_0$	$\bar{y}_1 y_0$	$y_1 y_0$	$y_1\bar{y}_0$
$\bar{c}$	0	1	1	0
c	×	×	×	×

$J_2 = \bar{y}_0$

	$\bar{y}_1\bar{y}_0$	$\bar{y}_1 y_0$	$y_1 y_0$	$y_1\bar{y}_0$
$\bar{c}$	×	×	×	×
c	×	1	1	×

$K_2=1$

	$\bar{y}_1\bar{y}_0$	$\bar{y}_1 y_0$	$y_1 y_0$	$y_1\bar{y}_0$
$\bar{c}$	0	0	×	×
c	×	0	×	×

$J_1=\bar{y}_0$

	$\bar{y}_1\bar{y}_0$	$\bar{y}_1 y_0$	$y_1 y_0$	$y_1\bar{y}_0$
$\bar{c}$	×	×	0	1
c	×	×	0	×

$K_1=\bar{y}_0$

	$\bar{y}_1\bar{y}_0$	$\bar{y}_1 y_0$	$y_1 y_0$	$y_1\bar{y}_0$
$\bar{c}$	1	×	×	1
c	×	×	×	×

$J_0=\bar{1}$

	$\bar{y}_1\bar{y}_0$	$\bar{y}_1 y_0$	$y_1 y_0$	$y_1\bar{y}_0$
$\bar{c}$	×	1	0	×
c	×	0	1	×

$K_2=1$

4.3. Down Counter

Divided-by-10 down counter

Divided - by - 10 Down Counter

The state diagram of ÷ 10 down counter is as follows :

There are 10 state, so no of FF is ld 10 = 4.

State Table

The state table of the counter may be obtained as shown in table :

	Present state				Next state		FF input	
Count	y_3	y_2	y_1	y_0	T_3	T_2	T_1	T_0
9	1	0	0	1	0	0	0	1
8	1	0	0	0	1	1	1	1
7	0	1	1	1	0	0	0	1
6	0	1	1	0	0	0	1	1
5	0	1	0	1	0	0	0	1
4	0	1	0	0	0	1	1	1
3	0	0	1	1	0	0	0	1
2	0	0	1	0	0	0	1	1
1	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	1

K-map

The excitation k-maps corresponding to T FFs are obtained as shown in Fig.

	$\bar{y}_1\bar{y}_0$	$\bar{y}_1 y_0$	$y_1 y_0$	$y_1\bar{y}_0$
$\bar{y}_3\bar{y}_2$	1	0	0	0
$\bar{y}_3 y_2$	0	0	0	0
$y_3 y_2$	X	X	X	X
$y_3\bar{y}_2$	X	0	X	X

$T_3=Y_2Y_1Y_0+Y_3Y_0$

0	0	0	0
1	0	0	0
X	X	X	X
1	0	X	X

$T_2 = Y_3\ \bar{Y}_0 + Y_2\ \bar{Y}_1\ \bar{Y}_0$

	$\bar{y}_1\bar{y}_0$	$\bar{y}_1 y_0$	$y_1 y_0$	$y_1\bar{y}_0$
$\bar{y}_3\bar{y}_2$	0	0	0	0
$\bar{y}_3 y_2$	1	0	0	0
$y_3 y_2$	X	X	X	X
$y_3\bar{y}_2$	1	0	X	X

1	1	1	1
1	1	1	1
1	1	1	1
1	1	1	1

$T_1=Y_1\ \bar{Y}_0+Y_3\ \bar{Y}_0+Y_2\ \bar{Y}_1\ \bar{Y}_0$

4.4. Exercise

4.4.1. Analytical questions

a) Obtain a odd sequence counter that produces the count sequence 1,7,3,5,2,6....

b) Obtain a synchronous counter that produces the count sequence 0,2,4,3,6,7,0.....

   i) prepare state diagram
   ii) prepare state table
   iii) k-map equation
   iv) circuit diagram.

c) What down you mean by down counter?

d) i) Design a divided by 7 down counter.
   ii) Design a divided by 16 down counter.