

Unit 4 : Sequential Machine

Lesson 1 : State Diagram and State Tables

1.1. Learning Objectives

On completion of this lesson you will be able to :

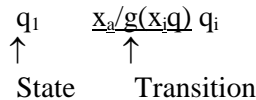
- ◆ define state diagram and state table
- ◆ know sequential machines and its types.

The functional interrelationship that exists among input, the output, the present state and the next state is best illustrated by the state diagram or state table.

1.2. State Diagram

The state diagram is a graphical representation of a sequential circuit.

The state diagram is a graphical representation of a sequential circuit in which the state are represented by circles and transitions between states shown by arrows. In another words, a state diagram consists of nodes interconnecting directed line segments corresponding to each state of the circuit.



If the corresponding to an input combination x_a , the present state of the machine q_i results in a next state q_j ; a line is drawn from q_i to q_j with an arrow directed towards q_j . The edge is labeled as $x_a/g(x_a, q_i)$.

Where $g(x_a, q_i)$ is the corresponding output of the machine resulting from the transition of the state q_i to q_j with input x_a .

Notes : The implementation of a sequential circuit with n states will require m FFs, where $2^m \geq n$. Say 3 states will require 2 FFs, since $2^2 \geq 3$, and output of the FFs are called the state variables which are used to identify which state the circuit is in.

1.3. State Table

The state table contains the same information as the state diagram in tabular form.

The state table contains the same information as the state diagram in tabular form. The transition table of a sequential machine shows the next state and output for all possible combinations of input and present state of the machine. This information are displayed in a table.

The state diagram can be drawn from FF control characteristics or excitation table. The control characteristics of various FFs are summarized below :

GY	SR	JK	D	T	
0 0	0 ×	0 ×	0	0	Excitation table
0 1	1 ×	1 ×	1	1	
1 0	× 1	× 1	0	1	
1 1	× 0	× 0	1	0	

So, the state diagram of S-R FF can be drawn from the above excitation table.

1.4. Sequential Machine

An abstract model of a sequential circuit is called a sequential machine.

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$$M = (X, Z, Q, f, g)$$

Where

X is a finite set of input symbols.

Z is a finite set of output symbols.

Q is a finite set of internal state.

f is a next state function, snapping from XxQ To Q.

g is a output mapping function, mapping from XxQ to Z.

Types of Sequential Machine

A sequential machine is of two types :

- ◆ Mealy machine
- ◆ Moore machine.

1.5. Mealy Machine

A sequential machine whose output are dependent on input (X) and present state (Q) is called a mealy machine.

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Output $Z = g(X, Q)$

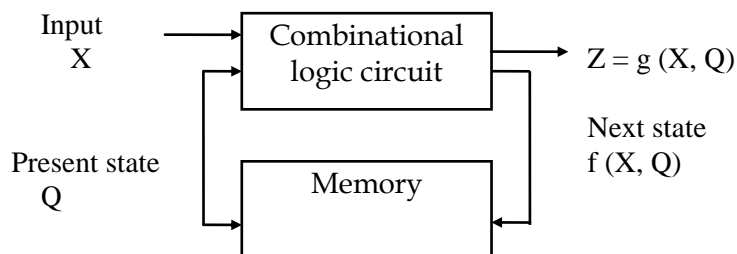


Fig. 4.1 : General model of mealy machine.

Sequential Machine

1.6. Moore Machine

A sequential machine whose outputs are dependent only on present state is called a Moore machine.

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Output $Z = g(Q)$
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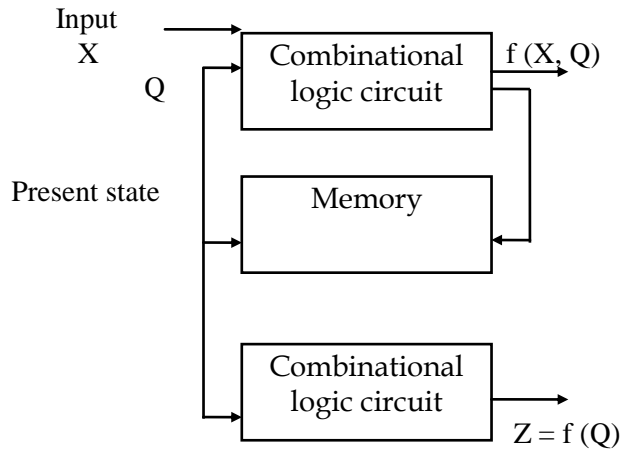


Fig. 4.2 : General model of Moore machine.

The transition table for Moore machine and mealy machine is as follows. For Moore machine $g(x, q) = g(q)$.

Table 4.1: Transition table for a Moore Machine.

Present State	Next State		Inputs		Output
	X1	X2	X1	X2	
q ₁	f(x ₁ , q ₁)	f(x ₂ , q ₁)	f(x ₁ , q ₁)	g(q ₁)
q ₂	f(x ₂ , q ₂)	f(x ₂ , q ₂)	f(x ₁ , q ₂)	g(q ₂)
...
...
q _k	f(x ₁ , q _k)	f(x ₂ , q _k)	f(x ₁ , q _k)	g(q _k)

Table 4.2: Transition table for a Mealy Machine.

Present State	Next State		Inputs	
	X1	X2	X1	X2
q ₁	f(x ₁ , q ₁), g(x ₁ , q ₁)	f(x ₂ , q ₁), g(x ₂ , q ₁)	f(x ₁ , q ₁), g(x ₁ , q ₁)
q ₂	f(x ₂ , q ₂), g(x ₂ , q ₂)	f(x ₂ , q ₂), g(x ₂ , q ₂)	f(x ₁ , q ₂), g(x ₁ , q ₂)
...
...
q _k	f(x ₁ , q _k), g(x ₁ , q _k)	f(x ₁ , q _k), g(x ₁ , q _k)	f(x ₁ , q _k), g(x ₁ , q _k)

The following example will clearly illustrate the sequential machine, state table and state diagram.

Examples

For sequential logic circuit with two inputs x_1, x_2 ; one output Z and two DFF type memory elements i.e.

Find the

- a) Transition table
- b) State table
- c) State diagram.

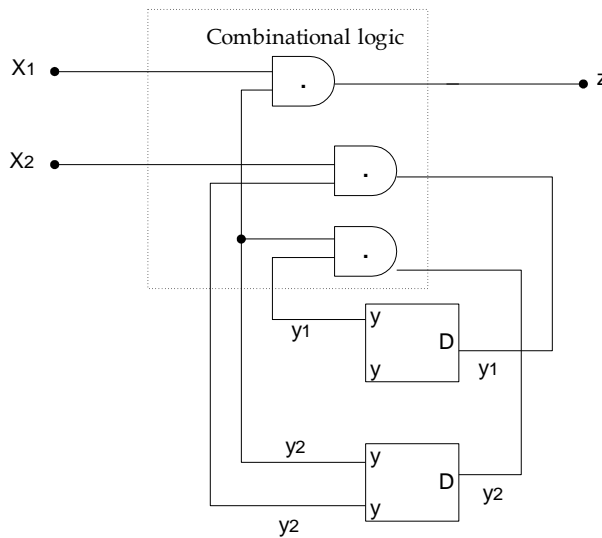


Fig. 4.3 : An example of sequential logic circuit.

Solution

From the circuit the output, excitation and next state functions of the FF can be written as

$$\begin{aligned}
 \text{Output } z &= g(x_1, x_2, y_1, y_2) \\
 &= x_1 y_2 \\
 \text{Next state equation } Y_1 &= f(x_1, x_2, y_1, y_2) \\
 &= (x_2 + y_2) \\
 Y_2 &= f(x_1, x_2, y_1, y_2) = y_1 y_2 \\
 \text{Excitation function } Y_1 &= D_1 = x_2 + y_2 \\
 Y_2 &= D_2 = y_1 y_2
 \end{aligned}
 \tag{1.1}$$

The transition table for the said machine of is shown in the following table.

Sequential Machine

Table 4.3 : Transition table for the sequential machine.

Present State y_1, y_2	Next State Y_1, Y_2				Output, Z			
	Input, x_1, x_2				Input, x_1, x_2			
	00	01	11	10	00	01	11	10
00	10	10	10	10	0	0	0	0
01	00	10	10	00	0	0	1	1
11	01	11	11	01	0	0	1	1
10	10	10	10	10	0	0	0	0

The entries in the table are made as follows :

Take for example the second row and third column corresponding to state $q_2 = 01$ and input symbol 11, we have $x_1=1, x_2=1, y_1=0, y_2=1$. From Eq.(1.1) we get $z=1, y_1=1, y_2=0$, therefore the table completed for all input symbols and present states.

Denoting state 00 by q_1 , 01 by q_2 ; 11 by q_3 and 10 by q_4 we can get the following state table 4.4 from transition table.

Table 4.4 : State table for the sequential machine.

Present state	Next state Q, Output Z			
	Input X = x_1, x_2			
	$X_1=00$	$X_2=01$	$X_3=11$	$X_4=10$
$q_1=00$	$q_4, 0$	$q_4, 0$	$q_4, 0$	$q_4, 0$
$q_2=01$	$q_1, 0$	$q_4, 0$	$q_4, 1$	$q_1, 1$
$q_3=11$	$q_2, 0$	$q_3, 0$	$q_3, 1$	$q_2, 1$
$q_4=10$	$q_4, 0$	$q_4, 0$	$q_4, 0$	$q_4, 0$

1.7. Exercise

1.7.1. Multiple choice questions

- a) The state diagram is a
 - i) diagrammatic representation of a sequential circuit
 - ii) graphical representation of a sequential circuit
 - iii) numerical representation of a sequential circuit
 - iv) graphical representation of a combinational circuit.

- b) How many types of sequential machine are there in this lesson?
 - i) 2
 - ii) 3
 - iii) 4
 - iv) 6.

- c) The outputs of mealy machine are dependent on
 - i) only present state
 - ii) input and present state
 - iii) output and next state
 - iv) present input and present output.

1.7.2. Analytical questions

- a) What do you mean by state table and state diagram?
- b) What is sequential machine? Briefly describe the different types of sequential machine.
- c) What are the main difference between Mealy machine and Moore machine?
- d) What is state variables? Write the sequential circuit implementation formula.

Lesson 2 : Analysis of Asynchronous Sequential Circuits

2.1. Learning Objectives

On completion of this lesson, you will be able to :

- ◆ analyze the asynchronous sequential circuit
- ◆ describe the critical race non critical race and Buzzer circle
- ◆ know the steps of analysis of Asynchronous sequential circuit.

2.2. Analysis of Asynchronous Sequential Circuits

In an asynchronous sequential logic circuit there is no clock or synchronizing pulses.

In an asynchronous sequential logic circuit there is no clock or synchronizing pulses. Each device in the system proceeds at a speed determined by its own physical design and characteristics.

Steps required to analyze the asynchronous sequential logic circuit are as follows :

Steps required to analyze the asynchronous sequential logic circuit

- ◆ Write the equation of excitation inputs of the Flip-Flops.
- ◆ Write excitation output of the Flip-Flops.
- ◆ Write the next state equation of the memory elements.
- ◆ Prepare transition table and state table from next state equations and output equations.
- ◆ Mark the stable states.
- ◆ Look for any critical race conditions or buzzer circles by analyzing the circuit for various input combinations.

Note : For a particular sequence of inputs, the output of the circuit can be determined. It can be noticed that when the input is changed, the operating point moves horizontally in the transition table. If an unstable condition results, the operating point will move vertically to the row whose present state is the same as the next-state entry which was previously obtained.

Example

Consider the asynchronous sequential circuit of Fig.4.4 using D-type memory elements. To analyze this circuit, first we have to determine the Boolean equations for the output and next state variables.

$$\begin{aligned}
 Y &= y_1 \bar{x}_1 + y_2 x_1 + \bar{y}_2 \bar{x}_1 \bar{x}_2 + y_1 x_1 \bar{x}_2 + y_2 \bar{x}_1 \bar{x}_2 \\
 Y_2 &= \bar{y}_1 x_2 + y_2 \bar{x}_1 + x_1 \bar{x}_2 \\
 Z_1 &= y_1 y_2 \\
 Z_2 &= y_1 y_2
 \end{aligned}
 \tag{2.1}$$

From the above equation (2.1) , a transition table can be prepared for the circuit as shown in the table 4.5.

Table 4.5: Transition table for the sequential machine.

Present state y_1y_2	Next state, $Y_1 Y_2$ Input, x_1x_2				Output z_1z_2
	00	01	11	10	
00	00	11	01	01	00
01	11	01	11	11	00
11	11	11	10	11	10
10	10	10	00	11	01

When $y_1y_2=Y_1Y_2$, then the circuit reaches a stable state and no further change of state occurs till the input is changed. The stable states are shown on the transition table by bold face numbers.

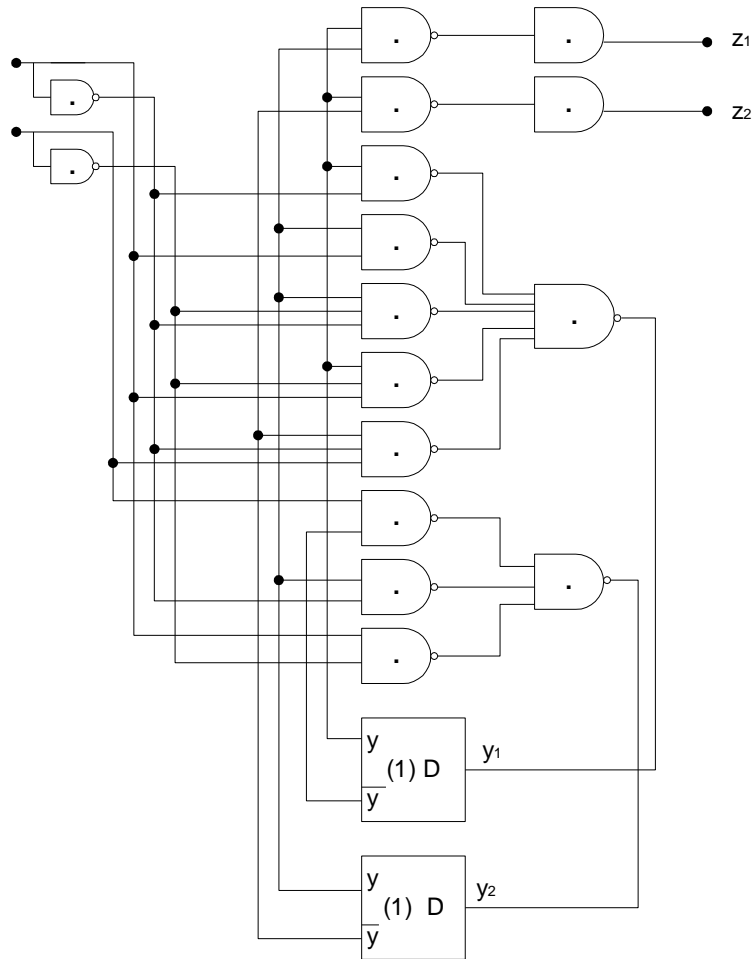


Fig. 4.4 : An asynchronous sequential circuit.

Sequential Machine

The operation of the sequential circuit can be studied from the transition table. Let us assume that the circuit is in stable state with 00/00 (x_1x_2/y_1y_2). Now if the input is changed from 00 to 10 ($x_1=1, x_2=0$), that leads to 10/01 after a delay of Δt seconds. Now 01 is not a stable state and taking as present state, the next state is obtained as 10/11 from the second row corresponding to state 01 and input 10. With 11 as the present state, the next state is also 11 and the circuit reaches its stable state **11**. The operation can be indicated as $00 \xrightarrow{\frac{\Delta t}{10}} 01 \xrightarrow{\frac{\Delta t}{10}} 11 \xrightarrow{\frac{\Delta t}{10}} 11$.

A change in input condition is allowed after a stable state has reached.

Consider the table 4.5 again with initial stable state 00/00. If the input is changed to 01, the next state, Y_1Y_2 , corresponding to this input change is 11 that the state of the first flip-flop which changes from 0 to 1 and second flip-flop state also changes from 0 to 1. Since two transitions takes place, relative timings of these changes become important. There are three possibilities :

- ◆ Second flip-flop changes its state earlier compared to first flip-flop. So, the states changes are $00 \xrightarrow{\frac{\Delta t}{10}} 01 \xrightarrow{\frac{\Delta t}{10}} 01$. This terminates in a final stable state **01**.
- ◆ First flip-flop changes its state earlier compared to second. State changes case are $00 \xrightarrow{\frac{\Delta t}{10}} 10 \xrightarrow{\frac{\Delta t}{10}} 10$ that leads to a stable state.
- ◆ Both the flip-flops change their states simultaneously to $00 \xrightarrow{\frac{\Delta t}{10}} 11 \xrightarrow{\frac{\Delta t}{10}} 11$. Out of these three possibilities only the last one is a valid transition for. So, than one flip-flops change their state, the final state is uncertain and depends upon the relative delays of various flip-flops. Such a condition is known as race condition. Race conditions are classified as critical (non-safe) races and non-critical (safe) races.
- ◆ Critical race condition is the one in which the stable state reached after the change in input depends upon the sequence in which the flip-flops change their state.
- ◆ Non-critical race condition is the one in which the final state remains same whatever is the sequence of change of flip-flop states. Another criteria of asynchronous sequential circuit is the existence buzzer circle in which the state of the circuit never reaches a stable state and goes on changing. As for example, starting with the initial state 00/00, the input is changed to 11,

this results in state change as $00 \frac{\Delta t}{11} 01 \frac{\Delta t}{11} 11 \frac{\Delta t}{11} 00 \frac{\Delta t}{11} 01$ and so on.

Note : In designing asynchronous sequential logic circuit care must be taken to avoid critical races and buzzer circles

2.3. Exercise

2.3.1. Multiple choice questions

- a) There is no clock or synchronizing pulses
- i) in an asynchronous sequential circuit
 ii) in an synchronous sequential circuit
 iii) in an combinational circuit
 iv) none of the above.
- b) For which case care must be taken to avoid critical races and buzzer circles
- i) in designing asynchronous sequential logic circuit
 ii) in designing synchronous sequential logic circuit
 iii) in designing combinational logic circuit
 iv) none of the above.

2.3.2. Analytical questions

- a) What do you mean by race condition? Describe the different types of race condition with example.
- b) What do you mean by buzzer circle?
- c) What are the steps of analyzing the asynchronous sequential circuit?
- d) Analyze the asynchronous sequential circuit and describe by the following next state and output equations.

$$Y_1 = x_1 x_2 + x_2 y_1 + y_1 \bar{y}_2$$

$$Y_2 = x_1 \bar{y}_1 + x_2 \bar{y}_1 + y_1 y_2$$

$$z = x_1 y_1 y_2 + x_2 y_1 y_2 + x_1 x_2 y_1$$

Lesson 3 : Analysis of Synchronous Sequential Circuits

3.1. Learning Objectives

On completion of this lesson, you will be able to :

- ◆ know the procedure of how to analyze the synchronous sequential circuit.

In asynchronous sequential circuit, there are two problems race condition and buzzer circle. But synchronous sequential circuit there is no possibility of occurring race condition and buzzer circle. Because in synchronous circuits, the changes in memory contents can occur only during the arrival of a clock pulse. In a synchronous circuit, each memory state lasts it least until the next clock pulse is applied and every state of the circuit is stable in between two clock pulses.

The analysis of synchronous sequential circuit is less complicated than that of asynchronous sequential circuits and the analysis can be performed through the following steps.

- ◆ write the equation of excitation inputs of flip-flop from combinational logic circuit.
- ◆ write the equation of excitation outputs of flip-flop from combinational logic circuit.
- ◆ write the next state equation of the memory elements.
- ◆ prepare transition table and state table from the next state and output equation.
- ◆ draw the state diagram from the state table.

Problem

Analyze the synchronous sequential circuit of Fig 4.5.

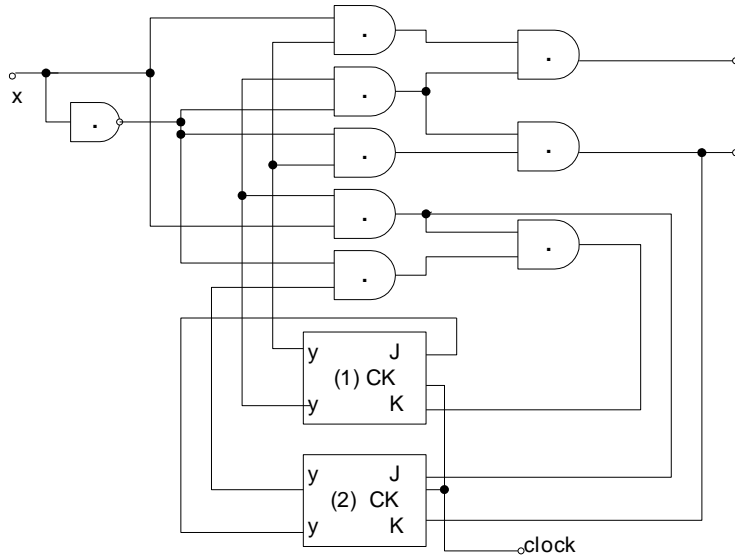


Fig. 4.5.

Solution : The excitations equations of the flip-flops are:

$$\begin{aligned}
 J_1 &= \bar{y}_2 \\
 J_2 &= y_1 x \\
 K_1 &= x \bar{y}_1 + \bar{x} y_2 \\
 K_2 &= x
 \end{aligned}$$

The output equations are :

$$z_1 = x y_1 + \bar{x} \bar{y}_1, z_2 = \bar{x}$$

The next-state equations for the JK flip-flops are :

$$\begin{aligned}
 Y_1 &= J_1 \bar{y}_1 + K_1 y_1 = \bar{y}_2 + x y_1 \\
 Y_2 &= J_2 y_2 + K_2 \bar{y}_2 = y_1 y_2 + x \bar{y}_2
 \end{aligned}$$

The transition table for the circuit is shown in Table 4.6.

Table 4.6 : Transition Table.

Present state $y_1 y_2$	Next state, $Y_1 Y_2$		Output, $z_1 z_2$	
	Input, x		0	1
00	10	11	11	00
01	00	01	11	00
11	00	11	01	10
10	10	10	01	10

Sequential Machine

Taking q_1 as 00, q_2 as 01, q_3 as 11 and q_4 as 10 as the states of the circuit. State table is shown in the table 4.7.

Table 4.7: State Table for the circuit.

Present state	Next state, Y_1Y_2		Output, z_1z_2	
	Input, x			
	0	1	0	1
q_1	q_4	q_2	1 1	0 0
q_2	q_2	q_2	1 1	0 0
q_3	q_1	q_2	0 1	1 0
q_4	q_4	q_4	0 1	1 0

From the state table, the state diagram can be prepared. The state diagram is shown in Fig. 4.6.

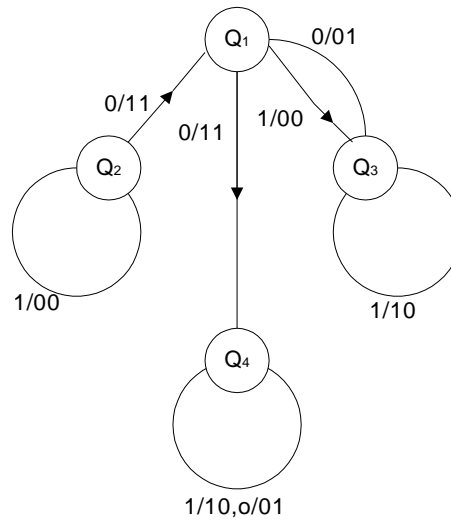


Fig. 4.6: State diagram for the circuit of Fig. 4.5.

3.2. Exercise

3.2.1. Multiple choice questions

- a) The problem in asynchronous sequential circuit is
 - i) race around condition
 - ii) buzzer circle
 - iii) race condition and buzzer circle
 - iv) none of the above.

- b) In synchronous circuits the changes in memory contents can occur only
 - i) when the $CK = 0$
 - ii) during the arrival of a clock pulse
 - iii) during the absence of a clock pulse
 - iv) none of the above.

3.2.2. Analytical questions

- a)
 - i) Why is the synchronous sequential logic circuits from form races?
 - ii) What are steps of analysis of synchronous sequential logic circuits?

- b) Analyze the following circuit by forming transition table, state table and transposition digital ram.

Lesson 4 : Design of Sequential Logic Circuit

4.1. Learning Objectives

On completion of this lesson, you will be able to :

- ◆ draw the flowchart of designing of a sequential machine
- ◆ know how to design a sequential circuit.

4.2. Design Algorithm

To design a sequential logic circuits, first we must have a precise description of the problem.

A comprehensive flowchart for the design of sequential machine.

To design a sequential logic circuits, first we must have a precise description of the problem. Then depending upon the requirements and the availability of other subsystems. We have to decide whether a synchronous or asynchronous operation as desired. The main steps in the design of sequential systems are listed below. Fig. 4.8 gives a comprehensive flowchart of an algorithm for the design of sequential machine.

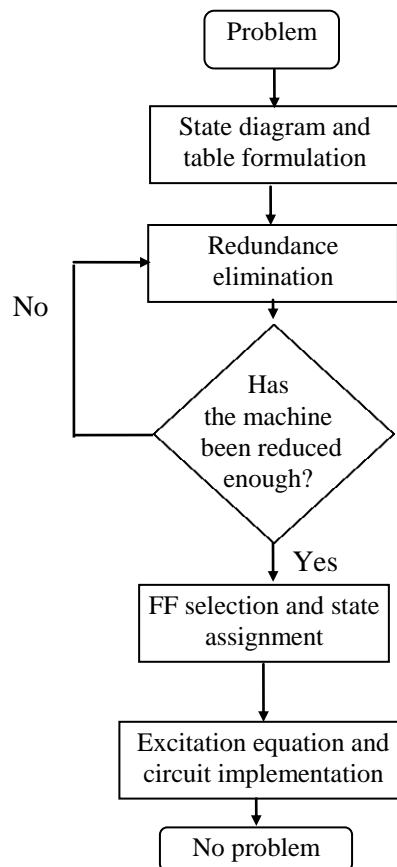


Fig. 4.7 : Sequential circuit design a flowchart.

The algorithm can be summarized by the following steps :

- Step 1.** Obtain the state diagram from the word statement of the problem.
- Step 2.** Obtain the state table from the state diagram.
- Step 3.** Eliminate the redundant states.
- Step 4.** Make state assignments.
- Step 5.** Determine the type of FFs to use and obtain the corresponding excitation maps.
- Step 6.** Determine the output and FF equations.
- Step 7.** Construct the logic circuit.

These design steps often lead to a rather lengthy process that varies from problem to problem.

The following examples illustrate the implementation of the sequential design algorithm.

Example :

Design a synchronous sequential circuit having a single input and single output. The output is to zero unless an input sequence 0101 is received.

Solution :

Step 1-2: To make a state diagram for this problem, we must begin with an initial state designated, as q_1 . (Fig.) Upon power-up, the circuit begins from state q_1 . As long as the string of input is devoid of 0 (i.e. first bit of 0101) sequence), the circuit remains at this beginning state once a 0 has been located the circuit moves to q_2 , indicating that the first bit has already been detected. Subsequent detection of 1,0 and 1; in that order, would amount to moving the circuit to states q_3 , q_4 and q_5 respectively once the stage q_5 is reached, the circuit gives an output indicating the completion of a 0101 sequence, while at state q_2 , if the circuit detects a 0, the circuit reenters state q_2 labeled as 0/0. This is due to the possibility that the most recently observed 0 might be the beginning of 0101 sequence. For similar reason, the detection of a 0 at state q_4 causes the circuit to move to state q_2 also. Again at state q_3 , a detection of 1 eliminates the possibility of having the desired sequence 0101. So, the circuit resets back to state q_1 . Like wise, the circuits resets from state q_5 to state q_1 if it locates a 1. However an interesting case happens when the circuit is at state q_5 and it has just detected a 1. This time the circuit moves back to state q_4 . This is due to the fact that detection of a at state W is equivalent to detecting the third bit of a newer 0101 sequence. The state table and state diagram are obtained as shown in Table 4.8.

Sequential Machine

Step 3: The problem involves 5 states requiring 3 FFs. Three of the eight possible states will remain unused.

Step 4: The state table and transition table corresponding to the arbitrary assignment of $q_1=000$, $q_2=001$, $q_3=010$, $q_4=011$, $q_5=100$ are shown in Table 4.9 and Table 4.10.

Step 5: The number of FFs are indeed 3. The output and excitation maps corresponding to the use of T FFs may now be obtained as shown below.

PS	NS, z	
	0	1
q_1	$q_2, 0$	$q_1, 0$
q_2	$q_2, 0$	$q_3, 0$
q_3	$q_4, 0$	$q, 0$
q_4	$q_2, 0$	$q_5, 1$
q_5	$q_4, 0$	$q_1, 0$

Table 4.8 : State Table.

PS			NS $y_1 y_2 y_3$		Output z	
y_1	y_2	y_3	$x=0$	$x=1$	$x=0$	$x=1$
0	0	0	001	000	0	0
0	0	1	001	010	0	0
0	1	0	011	000	0	0
0	1	1	001	100	0	1
1	0	0	011	000	0	0

Table 4.9 : Transition Table.

Y_1	y_2	y_3	T_1		T_2		T_2	
			0	1	0	1	0	1
0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	1	0	1
0	1	0	0	0	0	1	1	0
0	1	1	0	1	1	1	0	1
1	0	0	1	1	1	0	1	0

Table 4.10 : Excitation Table.

	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	×	×	×	×
10	1	1	×	×

$$T_1 = y_1 + y_2 y_3 x$$

	00	01	11	10
00	0	0	1	0
01	0	1	1	1
11	×	×	×	×
10	1	0	×	×

$$T_2 = y_1 x + y_3 x + y_2 y_3 + y_2 x$$

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	00	01	1	10
			1	
00	0	0	0	0
01	0	0	1	0
11	×	×	×	×
10	0	0	×	×

$$z = y_2 y_3 x$$

	00	01	1	10
			1	
00	1	0	1	0
01	1	0	1	0
11	×	×	×	×
10	1	0	×	×

$$T_3 = y_3 x + y_3 \bar{x}$$

Step 6: The excitation maps are minimized zero. Proper grouping of K-map cells results in the following equations.

$$T_1 = y_1 + y_2 y_3 x$$

$$T_2 = y_3 x + y_2 \bar{x} + \bar{y}_2 y_3 + y_1 \bar{x}$$

$$T_3 = y_3 x + \bar{y}_3 \bar{x}$$

$$z = y_2 y_3 x.$$

Step 7: The resulting circuit of 0101 sequence detector is obtained from these excitation equation.

4.3. Exercise

4.3.1. Multiple choice questions

- a) For designing a sequential logic circuit, we must have
 - i) a superficial description of the problem
 - ii) a precise description of the problem
 - iii) a solution of the problem
 - iv) none of the above.

- b) Which is the false statement?
 - i) The design steps of sequential circuit is fixed for all the problem.
 - ii) The design steps of sequential circuit varies from problem to problem.
 - iii) The design algorithm steps often lead to a rather lengthy process that varies from problem to problem.
 - iv) none of the above.

4.3.2. Analytical questions

- a) i) Draw the flowchart of designing sequential circuit/machine. ii) Write the algorithm of the said design.
- b) Complete the design of a clocked sequential circuit that recognizes the input sequence 1010, including overlapping such that for input $x = 00101001010101110$ the corresponding output z is 00000100001010000.
- c) Derive the state diagram and state table for synchronous sequential circuit having a single input and single output. The output is to be zero unless the input sequence of three consecutive 1's(111) occurs. Overlapping sequences are accepted for example if the input is 01011110 the required output is 00000110.

